REMARKS

Claims 15-20 remain pending in the present application of which claims 15, and 17-20 have been amended to more explicitly and more precisely describe the claimed invention. More specifically claim 15 has been amended to more precisely describe the claimed invention and claims 17-20 have been amended to correct some minor typo errors. Support for the amendments to claim 15 can be found on page 6, lines 22-23. Further, Applicant has also amended the title of the invention, and the abstract of the disclosure in order to correct some minor typo errors. It is believed that no new matter adds by way of the amendment made to the claims or otherwise to the specification. Reconsideration of these claims is respectfully requested.

DISCUSSIONS OF OFFICE ACTION REJECTIONS

Priority

1. The Office Action indicated that applicant has not filed a certified copy of the application as required by 35 U.S.C. 119(b).

A certified copy of the prior Taiwan application was submitted on June 21, 2002.

Objections to Specification

2. The Office Action objected to the abstract of the disclosure because "A thin film transistor" is an incomplete sentence.

In response thereto, Applicant has amended the Abstract of the Disclosure. After entry of the above amendments, it is believed that the above objects can be overcome. Reconsideration is respectfully requested.

3. The Office Action objected to the Title of the Invention as being not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

In response thereto, Applicant amended the title of the invention. After entry of the above amendment, it is believed that the above objections can be overcome. Reconsideration is respectfully requested.

Rejections under 35 U.S.C. 112

4. The Office Action rejected claims 17-20 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In rejecting the above claims, the Office Action asserted it is not clear what is meant by the following: "includes".

In response thereto, Applicant has amended claims 17-20. After entry of the above amendments, Applicant believes that the above rejections can be overcome. Reconsideration is respectfully requested.

Rejections under 35 U.S.C.§103

5. The Office Action rejected claims 15 and 16 under 35 U.S.C. 103(a) as being obvious over Applicant's Prior Art (hereinafter APA) in view of Wu et al. (US-5,977,561, hereinafter, Wu).

In rejecting the above claims, the Office Action asserted that the APA discloses an insulating substrate; a polysilicon layer over the substrate; and a gate structure over the polysilicon layer, wherein the gate structure includes a gate layer, a gate dielectric layer between the gate layer and the polysilicon layer. However, the APA fail to disclose a spacer on each side of the gate layer; and a conductive layer over the gate layer and the polysilicon layer adjacent to the spacers. Wu discloses a semiconductor device that has a spacer on each side of the gate structure; a conductive layer. It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the semiconductor device of the APA to include a spacer as described in Wu because it aids in isolating the gate, source/drain regions'; and a conductive layer in providing connection among the layers.

Applicant respectfully disagrees and traverses the above rejections as set forth below. Independent claim 15 is allowable over APA in view of Wu for at least the reason that substantially, APA and Wu fail to teach, suggest or disclose every features of the claimed invention. More specifically, APA and Wu fail to teach, suggest or disclose at least ***"a conductive layer over the gate layer and the polysilicon layer adjacent to the spacers, wherein***

the conductive layer adjacent to the spacers serves as a source/drain region, as required by claim 15." Because the above structure shows the formation of conductive layers over and adjacent of the gate structures in a selective and self-aligned manner, and also shows the use of the conductive layer as source/drain region, the efficiency and reliability of the device can be effectively promoted. Further, the above structure allows a much more simplified and cost effective method for manufacturing the claimed structure. Thus the cost of manufacturing can be substantially reduced and the through-put can be substantially increased.

To the contrary, the APA shows (FIG. 1B) a substrate (100) having a patterned polysilicon pad layer (102) thereon which is implanted with ions and annealed to serve as a source/drain region. An ultra thin polysilicon layer (104) on the upper surface and sidewalls of the polysilicon pad layer (102). A gate structure comprising an oxide layer and a polysilicon layer is disposed over the ultra thin polysilicon layer (104). It is clear that the APA shows that the ultra-thin polysilicon layer is formed over the sidewall and on the patterned source/drain region (104); and a gate structure is disposed over ultra-thin polysilicon layer. Whereas, the language in claim 15 of the claimed invention clearly recites that the source/drain is formed over the polysilicon layer, therefore, the APA cannot meet the claimed invention in this regard.

Further, as it is well understood by those skilled in the art that in order to form the patterned pad polysilicon layer (104) substantially requires masking, photolithography and etching process. Further in order for the patterned pad polysilicon layer to serve as a source/drain region, requires ion implantation and annealing processes. By contrast, the claim 15 requires ***"a conductive layer over the gate layer and the polysilicon layer adjacent to the spacers, wherein the conductive layer adjacent the spacers serves as a source/drain region.*** Since the claimed structure shows that the gate structure and the source/drain region are disposed over the (ultra-thin) polysilicon layer, and that the source/drain can be formed after forming the gate structure in a selective and self aligned manner, therefore, substantially, the masking, photolithography, etching, ion implantation and annealing processes required in the manufacture of APA structure can be effectively eliminated. Therefore the manufacturing cost can be substantially reduced and also the through put can be substantially increased. Further, because the claimed structure allows

the material of the source/drain can be formed from a low resistance material (claim 17-19), therefore, the operating speed of the device can be effectively increased.

The Office Action asserted that Wu discloses a semiconductor device that has a spacer on each side of the gate structure; a conductive layer. It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the semiconductor device of the APA to include a spacer as described in Wu because it aids in isolating the gate, source/drain regions'; and a conductive layer in providing connection among the layers.

Applicant respectfully disagrees and would like to point out that substantially, Wu shows a first conductive layer (34) adjacent the gate sidewall spacers (24) over the source/drain region, and a second conductive layer (26) over the gate. Accordingly, Applicant respectfully submit the combination still fails show the source/drain region over the ultra-thin polysilicon layer, ***and also most importantly fais to show the use of the conductive layer instead of the patterned pad polysilicon layer (104) to serve as a source/drain region.*** Accordingly, Applicant respectfully submits that no combination of APA and Wu can achieve the claimed invention.

For at least the foregoing reason, claims 15 and 16 patently define over APA and Wu. Reconsideration and withdrawal of these rejections is respectfully requested.

6. The Office Action rejected claim 17 under 35 U.S.C. 103(a) as being obvious over Applicant's Prior Art (hereinafter APA) in view of Wu and Kawachi et al. (US-6,104,040, hereinafter, Kawachi).

In rejecting the above claims, the Office Action asserted that the APA fail to disclose a the conductive layer includes an in-situ doped silicon germanium (SiGe) layer. However, Kawachi discloses a semiconductor device that has a thin film transistor with a SiGe conductive layer (col. 2, lines 51-55 and col. 7, lines 22-28). It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the APA to include a SiGe layer as disclosed in Kawachi because it aids in increasing the speed of the device.

As discussed above, APA and Wu fail to teach, suggest or disclose every features of the claimed invention as defined in claim 15. Kawachi et al. clearly fails to cure the deficiencies of APA and Wu. Accordingly, Applicant respectfully submits claim 15 is patentable over APA, WU and Kawachi for at least the same reasons set forth in paragraph 5 above. Claim 17 depends

from claim 15 and, thus, is also patentable for at least the same reasons as for claim 15. Reconsideration is respectfully requested.

7. The Office Action rejected claims 18 and 19 under 35 U.S.C. 103(a) as being obvious over Applicant's Prior Art (hereinafter APA) in view of Wu and Nakajima et al. (US-6,118,140, hereinafter, Nakajima).

In rejecting the above claims, the Office Action asserted that the APA fail to disclose the conductive layer is tungsten; the conductive layer is metal silicide. However, Nakajima discloses a semiconductor device that has a conductive layer of tungsten (col. 19, lines 4-10); the conductive layer metal silicide (col. 19, lines 4-10). It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the APA to include a tungsten or a metal silicide layer as disclosed in Nakajima because it aids in providing a connection among the layers.

Clearly, Nakajima cannot cure the specific deficiencies of APA and Wu as discussed in above paragraph 5. Accordingly, claim 15 is patentable over APA, WU and Nakajima. Claims 18 and 19 depend from claim 15 and, thus, are also patentable for at least the same reasons as for claim 15. Reconsideration is respectfully requested.

8. The Office Action rejected claim 20 under 35 U.S.C. 103(a) as being obvious over Applicant's Prior Art (hereinafter APA) in view of Wu and Gardner et al. (US-5,872,376, hereinafter, Gardner).

In rejecting the above claims, the Office Action asserted that the APA fail to disclose the spacer is a tetra-ethyl-ortho-silicate (TEOS) layer. However, Gardner discloses a semiconductor device that has a spacer comprised of TEOS. It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the APA to include a spacer layer of TEOS as disclosed in Gardner because it aids in isolating the gate, source and drain regions.

Clearly, Gardner cannot cure the specific deficiencies of APA and Wu. Accordingly, claim 15 patently define over APA, WU and Gardner for the same reason set forth in paragraph 5. Claim 20 depends from claim 15 and, thus, is also patentable for at least the same reasons as for claim 15. Reconsideration is respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 15-20 are in proper condition for allowance. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,
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Version with markings to show changes made

In the Title

The title of invention has been amended as follows:

[METHOD OF MANUFACTURING]THIN FILM TRANSISTOR HAVING A REDUCED SOURCE/DRAIN RESISTANCE

In the Abstract

The Abstract has been amended as follows:

A structure of a thin film transistor having a reduced source/drain resistance is disclosed. The thin film transistor [has]comprises an ultra thin polysilicon layer over a substrate, a gate structure that includes a gate layer, a gate oxide layer between the gate layer and the ultra thin polysilicon layer and a spacer on each sidewall of the gate layer, and a conductive layer over the ultra thin polysilicon layer and the gate layer adjacent to the spacers. A [selective deposition, such as an in-situ silicon-germanium deposition that utilizes the difference in properties between the spacer and silicon, is conducted to form the]conductive layer comprising a low resistance material is disposed over the gate layer, and over the ultra thin polysilicon layer adjacent the gate sidewall spacers, which conductive layer adjacent the gate sidewall spacers serves as a source/drain region.

In The Claims

Claims 15, and 17-20 have been amended as follows:

15. (Amended) A thin film transistor structure, comprising:

an insulating substrate;

a polysilicon layer over the substrate;

a gate structure over the polysilicon layer, wherein the gate structure includes a gate layer, a gate dielectric layer between the gate layer and the polysilicon layer and a spacer on each side of the gate layer; and

a conductive layer over the gate layer and the polysilicon layer adjacent to the spacers, wherein the conductive layer adjacent to the spacers serves as a source/drain region.

17. (Amended) The structure of claim 15, wherein the conductive layer [includes]comprises an in-situ doped silicon-germanium (SiGe) layer.

18. (Amended) The structure of claim 15, wherein the conductive layer [includes]comprises a tungsten layer.

19. (Amended) The structure of claim 15, wherein the conductive layer [includes]comprises a metal silicide layer.

20. (Amended) The structure of claim 15, wherein the spacer [includes]comprises a tetra-ethyl-ortho-silicate (TEOS) layer.